Amendments to the Claims:

1. 1.(currently amended) A codec comprising a programmed digital signal processor and an accelerator core in which computation of a coding algorithm is divided between the digital signal processor and the accelerator core, computationally relatively intensive parts of a coding algorithm being performed by the accelerator core, wherein the accelerator core includes a vector processor capable of processing multiple items of data simultaneously, said vector processor comprising a plurality of similar operational units capable of carrying out simultaneous data processing operations, said vector processor being operative to execute program instructions whereby a data processing operation is assigned for performance by one or more of the operational units on a plurality of data elements.

2. (canceled)

3. (canceled)

4. (currently amended) A codec according to claim 1 in which the vector processor [[structure]]has a single-instruction multiple-data architecture.

5.(currently amended) A codec according to claim 1 in which the vector processor [[structure]]has an instruction set that is optimised to perform encoding to a predetermined standard.

6.(original) A codec according to claim 5 in which the instruction set is optimised to perform CELP coding of speech signals.

7. (canceled)

8. (canceled)

9. (canceled)

10.(currently amended) A codec according to claim [[7]] 1 including a register bank, the operational units performing operations on data stored in the register bank.

11.(currently amended) A codec according to claim [[7]] 1 in which each operational unit can perform operations upon the output of one or more of the operational units.

12.(original) A codec according to claim [[7]] 1 in which each operational unit can store the result of an operation in the register bank.

13.(original) A codec according to claim [[7]] 1 in which an operation can be performed on the outputs of a plurality of the operational units to derive a further output value.

14.(original) A codec according to claim 13 in which the outputs of a plurality of the operational units can be summed.

15.(currently amended) A codec according to claim [[7]] 1 in which each operational unit can access a common memory unit.

16.(original) A codec according to claim 15 in which the common memory unit includes a ROM.

17.(original) A codec according to claim 15 in which the common memory unit includes a RAM.

18.(original) A codec according to claim [[7]] 1 in which each operational unit is a MAC unit.

19.(canceled)

20.(currently amended) A codec according to claim [[19]] 1 in which the program instructions are executed as microcode.

21.(original) A codec according to claim [[19]] 1 including a decoder by means of which the program instructions are decoded for execution by one or more operational units.

22.(original) A codec according to claim 21 in which the decoder includes a finite state machine.

23.(original) A codec according to claim 21 in which the decoder includes a programmed memory device.

24.(currently amended) A computer program product for defining a codec, the codec a programmed digital signal processor and an

accelerator core in which computation of a coding algorithm is divided between the digital signal processor and the accelerator core, computationally relatively intensive parts of a coding algorithm being performed by the accelerator core, wherein the accelerator core includes a vector processor capable of processing multiple items of data simultaneously, said vector processor comprising a plurality of similar operational units capable of carrying out simultaneous data processing operations, said vector processor being operative to execute program instructions whereby a data processing operation is assigned for performance by one or more of the operational units on a plurality of data elements.

25.(original) A computer program product according to claim 24 expressed in a hardware definition language.